A MILLIMETER WAVE PASSIVE FET MIXER WITH LOW 1/F NOISE

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ABSTRACT

A unique millimeter wave resistive FET mixer design provides down conversion to low IF frequencies with low 1/f noise. The single FET unbalanced mixer has a double sideband noise figure of 7.5 dB with a conversion loss of 9dB at an LO drive level of 9dBm. An RF to LO isolation of 15 dB is achieved through use of a resonant loop from drain to gate. The design allows downconconversion to low IF frequencies using a FET compatible process with a small chip size. A comparison of MESFET snf HEMT versions of the mixer shows that the 1/f noise level is higher in the HEMT mixer.

INTRODUCTION

FET based mixers have been investigated for many years with emphasis on active single or dual gate FET mixer designs. Drawbacks to the active FET mixer include high noise figure for the dual gate designs and poor 1/f noise characteristics at low IF frequencies for both single and dual gate designs. Recently passive FET based mixers have been reported by several authors [1,2] using the FET as a variable resistance element with no drain bias. Advantages of this approach include low 1/f noise, low dc power consumption and low intermodulation distortion. This paper describes a unique passive FET single ended mixer design in which the LO signal is applied to the gate of an FET while the RF signal is applied to the drain. The IF signal is taken from the source of the device. Since the IF frequency of the mixer is low, LO and RF frequencies cannot readily be separated by filtering. The design achieves isolation between the LO and RF ports by applying the signals at different terminals of the FET. Coupling between the drain and gate through the gate to source capacitance is minimized by forming a parallel resonant circuit with the capacitance. This approach has enabled us to demonstrate an LO to RF isolation of 15 dB. In addition, the MESFET based version of the mixer shows no evidence of 1/f noise over the 10 to 100 MHz IF frequency range included in this investigation. An HEMT version of the mixer design does show a 1/f noise component which increases with increasing LO drive.

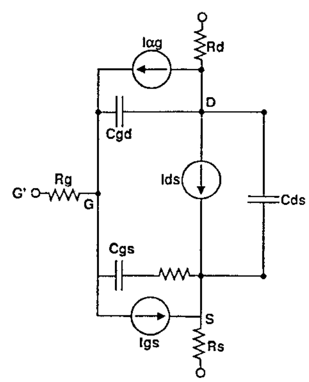
This single FET unbalanced mixer configuration provides performance comparable in many respects to a diode balanced mixer in the case where RF and LO frequencies are only slightly separated and the IF frequency is low. Diode balanced mixers based on FET implants evaluated in our laboratory differ from the FET mixer mainly in a lower LO drive requirement for the diode mixer. On the other hand, the balanced diode mixer chip occupies an area of 6.2 mm^2 compared to 1.9 mm^2 for the FET mixer.

DESIGN

Design and simulation of the mixer performance was done using the CAD program LIBRA. Initial values of RF and LO matching network elements and the gate to drain resonant circuit element are selected using a small signal circuit model. Large signal simulations using the Curtice FET model shown in Figure 1 are performed to arrive at the final values and to simulate conversion loss. Parameter values used in the model were based on estimates made from DC and small signal S parameter measurements.

Rs	6 ohms
Rd	6 ohms
Rg	10 ohms
Cgs	.04 pF
Cds	.05 pF
Cgd	.04 pF
α	1.3 V^{-1}
β	30×10^{-3} A/V^2
λ	0
V_{TO}	-2.7 V

$$I_{ds} = \beta(V_{GS} - V_T)^2 \; (1+\lambda V_{DS}) \; \tanh(\alpha V_{DS})$$



Curtice Asymmetric Model

Model Parameters for Non Linear FET Model

FIGURE 1 - FET Model Used in LIBRA Simulations

A photomicrograph of the mixer IC is shown in Figure 2. Dimensions of the MMIC are 1.04 mm x 1.72 mm x 0.1 mm. The mixer is designed around a 0.25 micron by 200 micron interdigital FET with four gate fingers. IF output of the mixer is taken from the source terminal of the FET through a filter designed to produce a virtual ground at the source terminal for the LO and RF frequencies. The LO and RF signals are applied to the gate and drain respectively through appropriate matching networks. A loop of high impedance line from drain to gate provides improved RF to LO port isolation. DC shorting of drain to gate is prevented by placing a blocking capacitor in series with the line. The mixer has been fabricated on both ion implanted material and MBE grown HEMT structures.

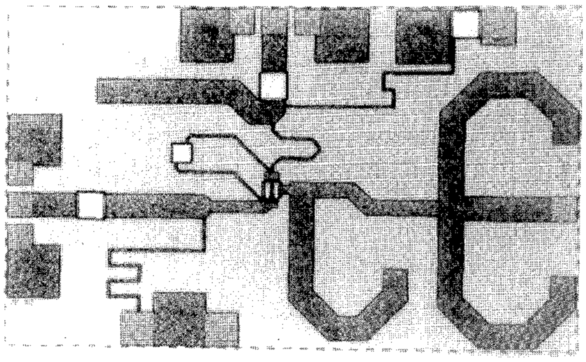


FIGURE 2 - Photomicrograph of Passive FET Mixer (chip size is 1.04mm x 1.72mm x 0.1mm)

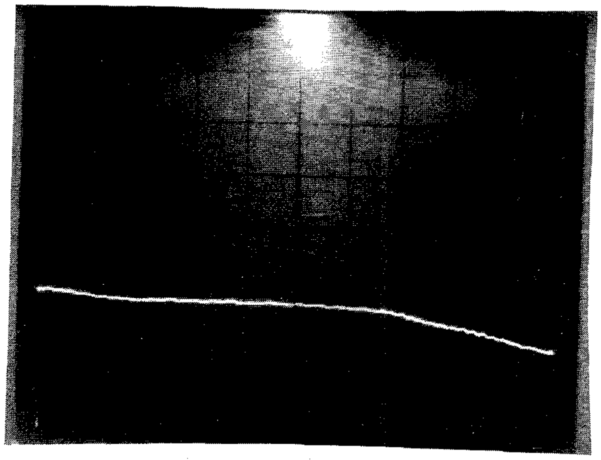
In actual operation the drain of the mixer FET mixer is biased at zero volts. The gate is biased with negative gate voltage to a value somewhat less negative than the pinch-off voltage for maximum transconductance.

FABRICATION

Both MESFET and HEMT versions of the mixer were fabricated using a hybrid stepper/e-beams lithography process on 3 inch wafers. The MESFET version used a Si^{29} implant at 100 keV with a $7e^{12}cm^{-3}$ dose for channel doping and a buried Be^{9} implant at 80 keV with a dose of $6e^{11}$ cm^{-3} to improve the implant profile. The HEMT version is a standard $Al_xGa_{1-x}As/GaAs$ structure with an x value of 0.22. Backside processing includes thinning wafer to 4 mils, reactive ion etching of through substrate via holes, backside gold plating and etching of streets in the gold plating for chip separation.

PERFORMANCE

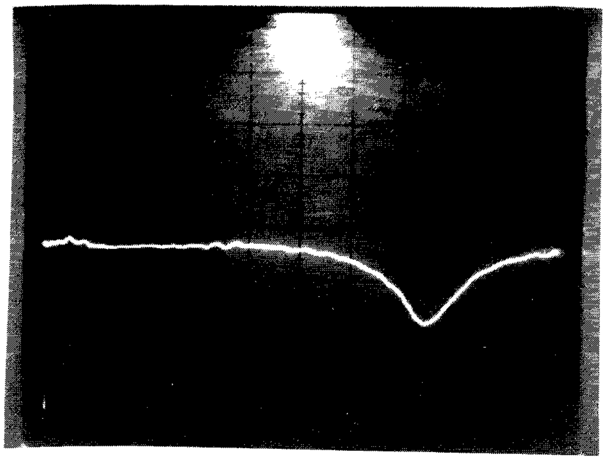
For RF evaluation the mixer MMIC was mounted in a test fixture with waveguide inputs for the LO and RF signals and a coax connector for the IF output. The IF output is fed to an IF amplifier with 30 dB gain and a 1.2 dB noise figure. RF and LO signals are coupled to the mixer through a finline waveguide to microstrip transition. The measured LO port return loss and LO to RF isolation are shown in Figures 3 and 4. The LO port return loss is greater than 10 dB over a 1.5GHz band centered at 34.5GHz. RF to LO isolation is better than 15 dB over the same frequency range. Double sideband noise figure and conversion loss as a function of IF frequency are shown in Figure 5 for a range of LO drive levels from 7 to 15 dBm. Fixture losses of about 1dB are included in the measured data. With 9dBm of LO drive the double sideband noise figure is 7.5 dB and conversion loss is 9dB. At higher LO drive levels the noise figure drops by 0.5 dB and the gain increased by about the same amount. The conversion loss calculated by LIBRA with the Curtice FET model was 9 dB with a 9dBm LO drive.



Horizontal f-27 to 37 GHz
Vertical 10 dB/div
Center Line 0dB

FIGURE 3 - LO to RF Isolation vs. Frequency

A ALGaAs/GaAs HEMT version of the mixer was also fabricated and tested. No circuit modifications were made to account for differences in devices, but rather the HEMT was simply incorporated into the existing MESFET design. Measured conversion loss and noise figure data shown in Figure 6 indicate several interesting differences between the two mixers. At the high end of the IF frequency range the mixers ultimately reach a noise figure of 6-7 dB accompanied by a conversion loss of 5-6 dB. However the HEMT requires less LO drive to reach a saturation point. The lowered LO drive requirement would be expected due to the lower threshold voltage and increased transconductance of the HEMT. On the other hand, the HEMT mixer shows evidence of a 1/f noise component at lower IF frequencies that becomes increasingly prominent at higher LO drive levels. The increased noise is undoubtedly due to trapping of carriers injected at the gate contact.



Horizontal f-27 to 37 GHz
Vertical 10dB/div
Center Line 0dB

FIGURE 4 - LO Port Return Loss vs. Frequency

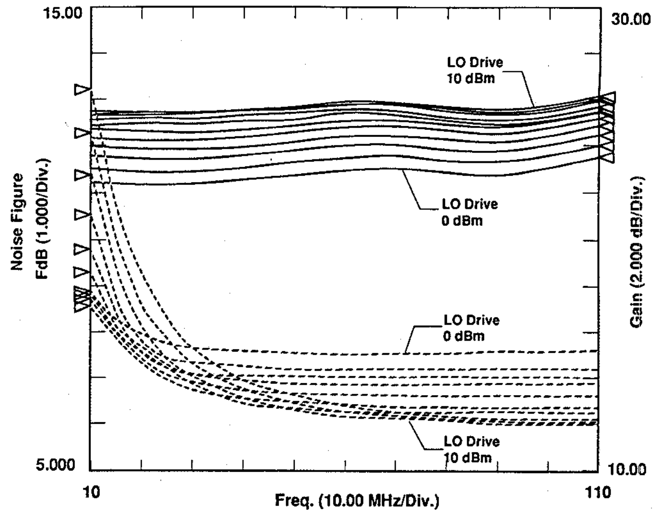


FIGURE 6 - Noise Figure and Conversion Loss for HEMT Mixer with LO Drive Levels of 0 to 10 dBm.

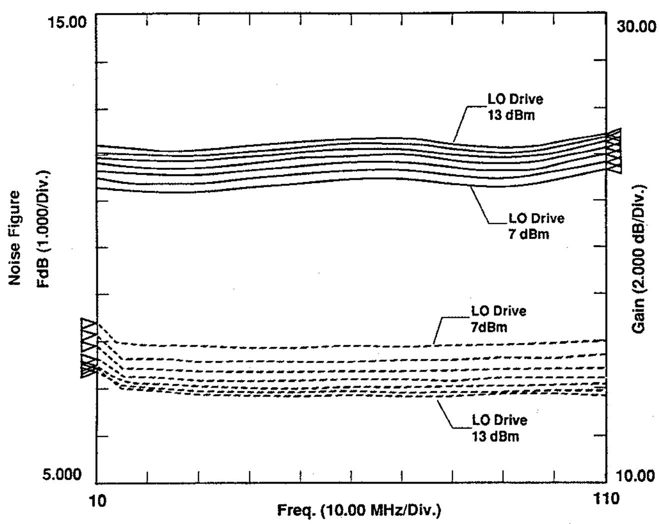


FIGURE 5 - Noise Figure and Conversion Loss for Implanted FET Mixer with LO Drive Levels of 7 to 13 dBm.

CONCLUSIONS

The unique mixer design demonstrated here provides a simple FET compatible approach for mixers with low IF frequency requirements. The lower frequency limit due to 1/f noise depends on the device technology used in fabrication. If standard MESET technology is used the 1/f noise corner is less than 10 MHz. Use of HEMT technology can move the 1/f noise corner to higher frequencies in the 10 to 30 MHz range depending on LO drive.

ACKNOWLEDGEMENTS

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